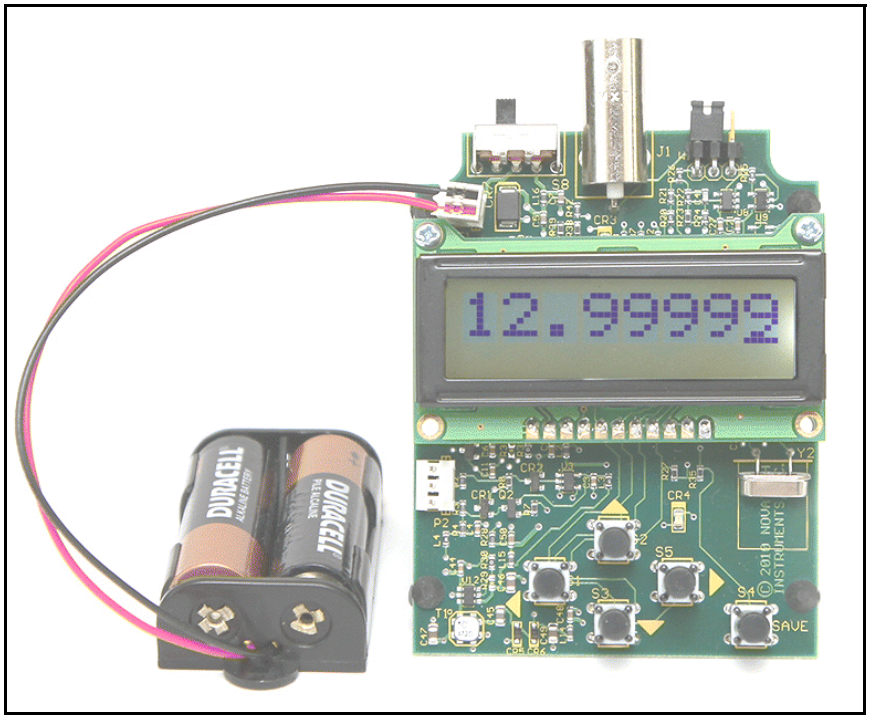
NOVATECH
INSTRUMENTS, INC.

INSTRUCTION MANUAL

Model 101A 12MHz DDS Signal Generator Module



101A shown with battery power

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1.0 DESCRIPTION

1.1 The Model 101A is a **D**irect **D**igital **S**ynthesized (DDS) signal generator on a small circuit board module with either serial or front panel control. The 101A provides a sine wave or an LVCMOS output signal that can be set from 10 Hz to 12.99999 MHz in 10 Hz steps in one continuous range.

1.2 Five front-panel push buttons, in conjunction with the eight-digit liquid crystal display (LCD), allow setting of the frequency. A jumper is provided to select between a sine output (a triangle wave is selectable via the serial port) and an LVCMOS output. Both have nominal 50Ω output impedance.

1.3 For embedded applications, consult the factory for the availability of a through-hole component free board. This allows the module to be installed on a customer application board.

2.0 SPECIFICATIONS

2.1 OUTPUT
TYPES: Sine or LVCMOS.
IMPEDANCE: 50Ω.
RANGE: 10 Hz to 12.99999 MHz with 10 Hz resolution in one continuous range.
AMPLITUDE: Sine: approximately 1.0 V_{pp} into 50Ω, typ. ±2dB from 1 MHz level. Audio level: typ. ±0.1dB from 20 Hz to 100 kHz. LVCMOS: 2.4 V_{oh}, 0.4 V_{ol} O.C., series terminated, 50Ω output. t_r, t_f <2 ns.

2.2 CONTROL
Five front-panel push buttons and display allow setting of output. Eight character LCD shows frequency in MHz, with 10 Hz resolution. RS232 (approximately ±3 V levels) serial port at 9600 Baud can be used without the display or the push buttons. The Save button, or serial Save command, stores instrument settings in EEPROM. This allows the 101A to be pre-programmed for embedded applications.

2.3 SPECTRAL PURITY (50Ω load, 25 MHz span, Sine Output)
Phase Noise: <-100dBc, 10 kHz offset, 1 MHz out.

Spurious: <-50dBc below 1 MHz
<-40dBc below 5 MHz
<-30dBc below 12 MHz

Harmonic: <-55dBc below 1 MHz
<-45dBc below 5 MHz
<-35dBc below 12 MHz

2.4 ACCURACY AND STABILITY
Accuracy of ±0.005% at 20°C and a stability of ±0.0025% from +5 to +40°C.

2.5 POWER REQUIREMENTS
DC Input: nominal +2.8 V_{dc} (2.0-3.0V_{dc}) at <100mA. Two LR6 (AA) alkaline cells (holder supplied) will power the Model 101A for at least 10 hours of operation.

2.6 SIZE
80mm L, 61mm W, 12mm H. excluding connectors. An additional 10mm is added to the height when the display is attached. Mounting holes and rubber feet provided.

2.7 ENVIRONMENTAL
Temperature: +5°C to +50°C operating. Humidity: 80% to 31°C, decreasing linearly to 50% at 40°C.

2.8 CONNECTORS
BNC for output. Jumper to select Sine or LVCMOS. 2-pin header for DC input. 3-pin header for RS232. A through-hole component (push buttons, connectors, and switches) free version is available for OEM applications (consult factory).

3.0 HARDWARE SETUP

WARNING:

The components on the 101A are static sensitive. Use static-aware handling procedures when operating the module.

3.1 The notes in this section apply to the Model 101A with installed display

3.2 **Power Connection.** The required power of +2.8 Volts DC is applied through a 2-pin header, BT1. The positive lead is on Pin 1 (the pin closer to the center of the board).

3.3 The quality of your power supply may affect the performance of the 101A. The supply should be free

of ripple and noise (<50 mV). Even though extensive filtering is used internal to the 101A, a quiet and well regulated power supply will ensure optimum performance.

WARNING:

While the power input is over-voltage and reverse-voltage protected, sustained overloads may damage the board.

NOTE:

Common digital supplies of 2.5 or 2.8 Volts, with appropriate filtering, are good choices for the 101A. Linear regulation from a 3.3 Volt digital supply down to a 2.8 Volt level is another good choice.

3.4 **Power on reset.** After power is applied, the 101A takes approximately 2 seconds to initialize. Commands or button presses (except Save being held down) during this time will be ignored or may cause erroneous operation.

3.5 **Signal Outputs.** There is one signal output. Connect your 50Ω application cable to the BNC output receptacle.

3.6 **Power Up.** To use the 101A, connect your power to BT1, and slide the switch to the ON position (toward the center of the board). An LED, CR4, will illuminate to indicate power is applied and on.

3.7 **Front Panel Operation.** Use the Left and Right buttons to select the digit you wish to modify. Then use the Up and Down buttons to modify that digit. The digit values will carry or borrow as necessary. The firmware will not allow you to increment or decrement a digit if the action will result in an out-of-limit value of greater than 12.99999 MHz or less than 10 Hz.

3.8 You can use the Save button to store the present settings into EEPROM. These settings will be used upon next reset or power cycle. The backlight will momentarily blink to indicate that the settings have been saved.

3.9 If you wish to clear saved values, hold down the Save button while sliding the power switch to the ON position. Then release the button. The Model 101A will then re-initialize with the factory default frequency of 100 kHz, and cursor in the 100 Hz position.

3.10 Jumper, W1, is provided to select between sine or LVCMOS outputs. For sine, place the shunt over the two pins closer to the center of the board. For LVCMOS, move the shunt to the two outer pins.

3.11 To conserve power, especially important in battery powered applications, the backlight will illuminate only after a command or a button push. It will stay illuminated for approximately 15 seconds.

3.12 The board monitors its input voltage. If the voltage drops below approximately 2 Volts, the digit at the present cursor position will blink.

3.13 **Mounting.** The 101A board provides mounting holes suitable for use with #4 or 2.5mm screws. The holes are connected to circuit common (ground). As provided, these holes have rubber mounting feet installed. Clip them out if you wish to mount your board. A clearance of 3mm (0.125 inch) is necessary if a metal or other conducting substrate is used. See Figure 2 for hole locations.

4.0 Serial Operation

4.1 If you are using a computer, terminal or other control source, please note that the data **FROM** the 101A is on pin 1; the data **TO** the 101A is on pin 2 and the **COMMON** return is on pin 3. Set your host to 9600 Baud, 8 bits, 1 stop bit, no parity and no hardware flow control. See Table 1 for Serial Commands.

4.2 The levels on the serial port are approximately ±3 V. These do not conform with RS232 specifications, but are adequate for short cable runs and are compatible with most computers or adapters.

4.3 You may use an USB to Serial adapter with computers that do not provide a serial port. Follow the manufacturer's installation instructions when using a USB adapter.

4.4 Commands are not case sensitive. The commands `R`, `CLR`, `S`, `V`, and `QUE` do not require any operand. End with any combination of `CR`, `LF` or

Table 1: Serial Commands

Serial Command	Function
`F0 xx.xxxxx`	Set Frequency of output in MHz to nearest 10 Hz. Decimal point required. Maximum setting: 12.99999 MHz.
`E x`	Serial Echo control. x=D for Echo **D**isable, x=E for Echo **E**nable
`R`	Reset. This command resets the 101A. EEPROM data is preserved and, if valid, is used upon restart. This is the same as cycling power.
`CLR`	Clear. This command clears the EEPROM valid flag and restores all factory default values. This is the same as holding the SAVE button down during power-up
`S`	Saves current state into EEPROM and sets valid flag. State used as default upon next power up or reset. Use the "`CLR`" command to return to default values..
`QUE`	Return present frequency, status registers, and software revision.
`M x`	Mode command. x=S for **S**ine wave output (default). x=T for **T**riangle wave output.
`V`	The V command returns a single byte representing the raw input voltage. Nominal 2 V cutoff is 0x9A. Scale factor is approximately 13mV/count.

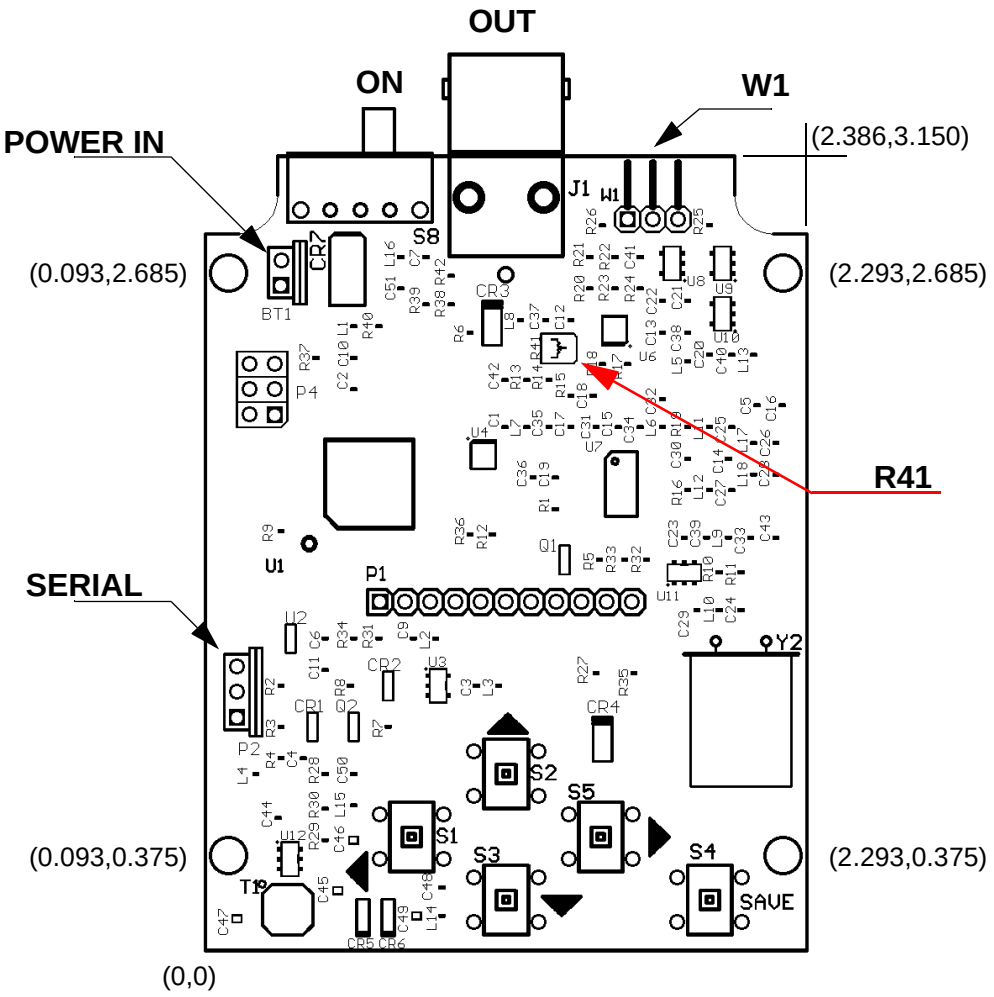


Figure 2: Top View, without Display

CRLF. The user host computer software must properly format the serial commands. Improper commands will result in an error code being returned per Table 2.

4.5 The "QUE" command returns a character stream showing current frequency, status registers and software revision. See page 7 for an explanation of the values that make up this string.

Table 2: Serial Error Codes

Error Code	Meaning
OK	Good command received
?0	Unrecognized Command
?1	Bad Frequency
?3	Input line too long
?6	Bad Mode
?8	Bad Constant
?f	Bad Byte

4.6 After the 101A has been installed in the customer application system, all that is required for operation is to send the appropriate serial commands per Table 1.

4.7 For maximum interface speed, it is suggested that Echoing be disabled by the "E d" command. This will allow the host to send characters at a faster rate. No flow control is used. Depending upon your host, the 101A may not be able to keep up with serial characters. You will have to verify correct operation at your host rate.

4.8 Use of the serial port does not disable the front panel interface. You may use any combination of button pushes or serial commands to control the 101A. Be sure not to issue commands simultaneously with operating the front panel interface.

5.0 Theory of Operation

5.1 Please refer to the simplified System Block Diagram in Figure 3 for the following discussion.

5.2 At every cycle of the 101A master clock, the 28-bit DDS integrated circuit increments the phase of an internal register by a value determined by the frequency setting loaded into the on-chip registers. This digital phase value is converted on-chip to a digital sinusoidal amplitude level and delivered to an on-chip 10-bit digital-to-analog converter.

5.3 The frequency generated by the DDS IC is determined by the 28-bit frequency word loaded into the frequency registers on the 101A. This value is calculated from either the front panel set value, or the value sent via the serial port. The display will always show the present output frequency.

5.4 Since the DDS IC is a sampled data system, the output frequency is limited to a maximum of 1/2 the master clock frequency ($F_{DDS} <= 2^{28}$-1). While it is possible to generate an output near 50% of the clock, the distortion may be unacceptable. Therefore, the output is limited to approximately 30% of the system clock and a sharp cutoff output filter is provided on board: in this case a differential 5th-order elliptical low pass filter.

5.5 The output of the differential filter is amplified and converted to a single-ended sine wave. This sine wave is simultaneously shifted to LVCMOS logic levels. Either the sine wave or the LVCMOS signal is selected by the jumper, W1.

5.6 The waveform selected by W1 appears on the center conductor of the output BNC receptacle.

6.0 PERFORMANCE TEST

6.1 Operate the 101A as directed in Section 3 or 4. The test limits assume a stable environment of 18-28^{o}C.

6.2 See Table 3 for a list of recommended test equipment to perform the following measurements.

Table 3: Recommended Test Equipment

Item	Minimum Specification	Recommended
Oscilloscope	100MHz, 50Ω	Tektronix TDS3032B
50Ω Termination	50Ω, ±1%	Tektronix 011-0049-01

Table 3: Recommended Test Equipment

Item	Minimum Specification	Recommended
Frequency Counter	25MHz	HP53132A
Counter Time Base	10MHz, <±0.1ppm	Novatech Instruments Model 2960AR

NOTE:

Allow the 101A to warm up for at least 5 minutes before performing any measurements. For best results, the 101A should be verified in its installed environment.

6.3 **Verify Frequency Accuracy.** To verify the frequency of the 101A, set the output sequentially to each value in Table 4. Connect the recommended frequency counter set to 50Ω termination and 1Hz resolution. Verify the limits show in Table 4. If you do not use an external reference for the frequency counter, be sure to compensate for the accuracy of your counter. (LSD = **L**east **S**ignificant **D**igit on counter).

Table 4: Frequency Test Points

Frequency	Tolerance
1 kHz	±0.05 Hz ±1 LSD
10 kHz	±0.5 Hz ±1 LSD
100 kHz	±5.0 Hz ±1 LSD
1 MHz	±50 Hz ±1 LSD
12 MHz	±600 Hz ±1 LSD

6.4 **Sine Out Amplitude Verification.** Set the frequency of the 101A to 1 MHz. Connect the 101A to the oscilloscope set for 50Ω termination. Set the oscilloscope to measure to amplitude using at least 16 averages. Verify a reading of $1V_{pp}$ $\pm 0.25V_{pp}$.

6.5 **Output Flatness Verification.** Verify that the sine amplitude is flat with frequency by connecting the 101A to the oscilloscope set for 50Ω termination. Note the voltage amplitude reading at 1 MHz.

6.6 Set the 101A to the values of Table 4. Verify that the oscilloscope amplitude reading remains within ±2dB (x1.26 to x0.79) of the value noted in the previous paragraph.

6.7 **LVCMOS Verification.** Verify the LVCMOS output is within specifications by performing the following test: Connect the 101A to the oscilloscope set for 50Ω termination. Use the same settings as Sine Out Amplitude Verification. Verify that the output has 30 to 70% duty cycle.

6.8 To verify the LVCMOS amplitude, set the frequency to 1 kHz. Set the oscilloscope for a 1 MΩ input impedance. Verify V_{oh}>2.4 V and V_{ol}<0.4 V.

6.9 This concludes the verification test of the Model 101A.

7.0 CALIBRATION

7.1 The 101A has only one adjustable component: R41, output amplitude. Calibration should be performed only if the 101A fails the performance test or if the unit has been repaired. Routine adjustment is not recommended nor generally required.

WARNING:

Access to R41 requires that the display be removed before supplying power. Calibration should be performed only by qualified personnel. You may save the frequency value of 1 MHz rather than using the serial port.

NOTE:

Allow the 101A to warm up for at least 15 minutes before performing any adjustments. For optimum performance the 101A should be calibrated in an environment similar to its installation.

7.2 **Amplitude Adjust, R41.** Set the oscilloscope to measure amplitude, with a minimum of 16 averages and 50Ω termination. Set the output to 1 MHz by sending the command `"F0 1.00"` or use the save button before removing the display. Adjust R41 for 0.9 V_{pp} to 1.1 V_{pp}.

7.3 Turn off the power. Replace the display and its hardware.

7.4 This completes the calibration of the Model 101A.

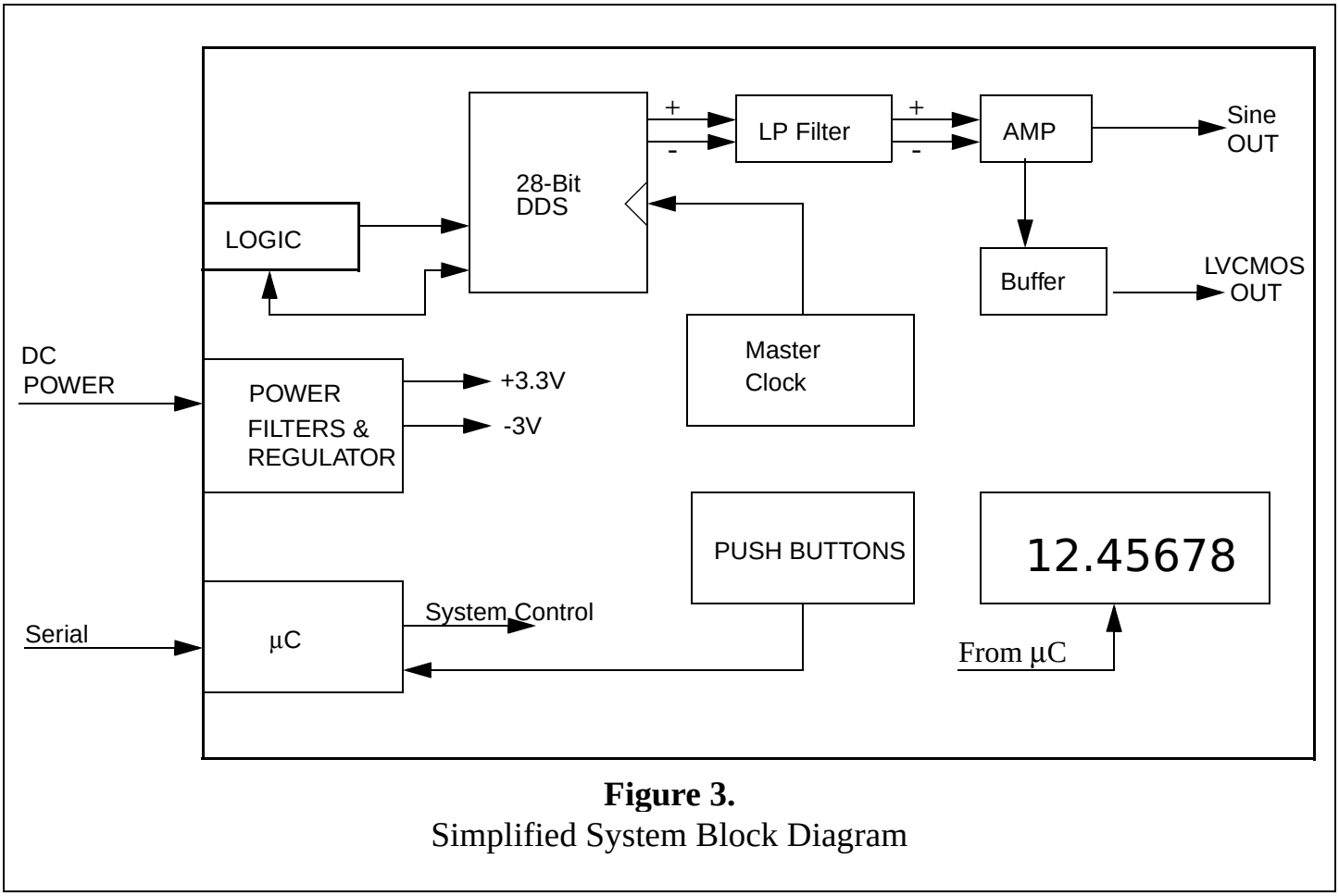


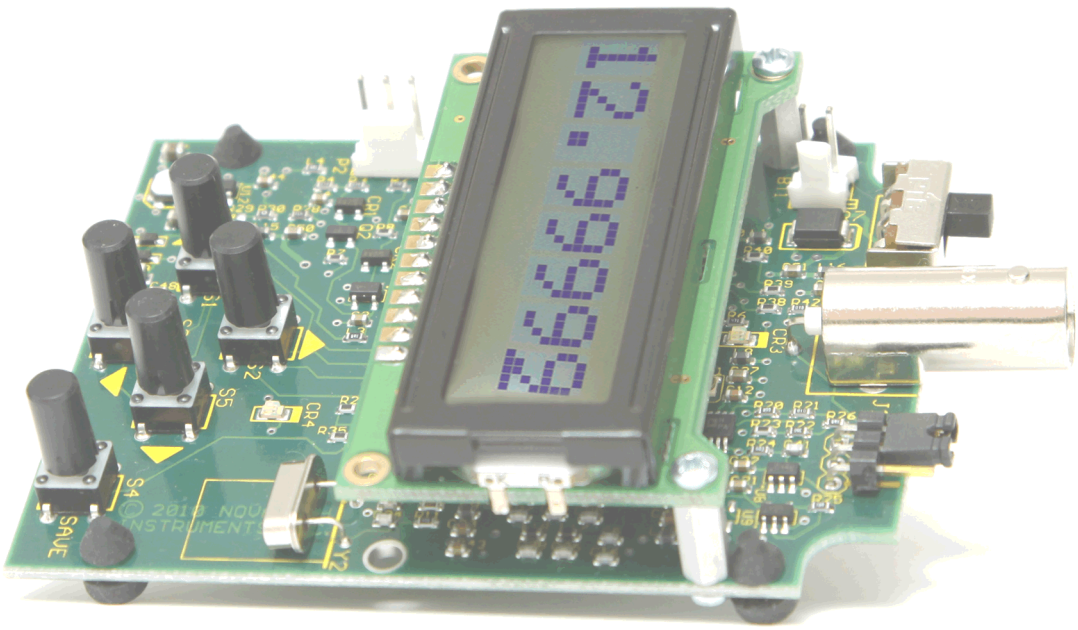
Figure 3.
Simplified System Block Diagram

"Que" command returns the following string of output values:

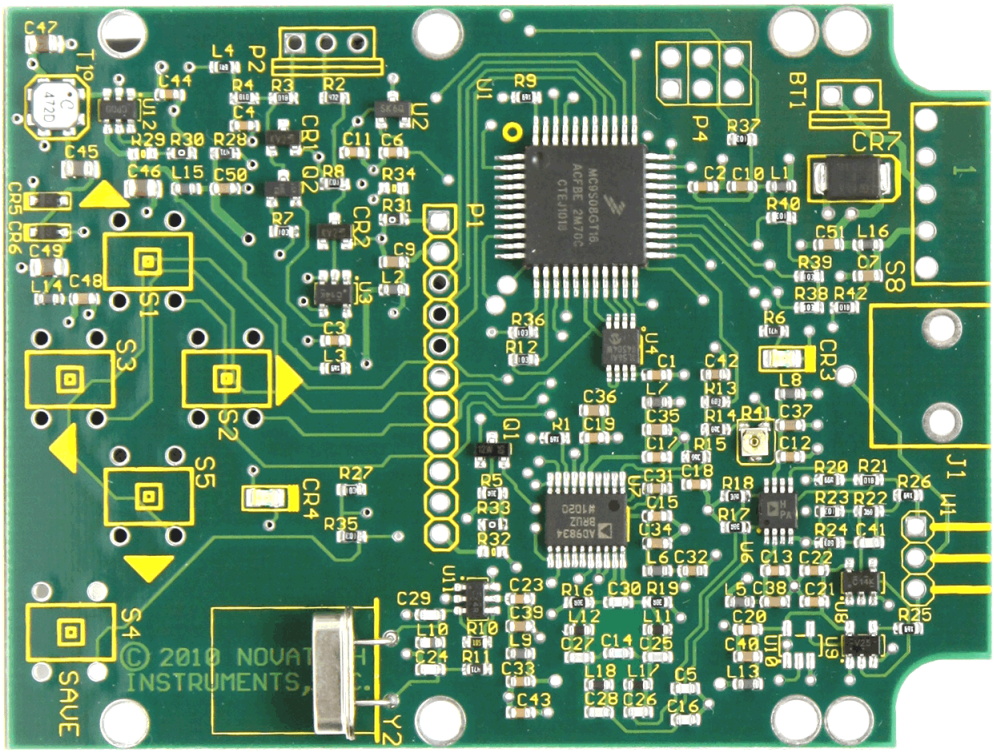
```
01245678 2008 10
```

Description:
"01245678", frequency in 10 Hz steps per least significant digit; "2008", internal control registers; "10", software revision number as X.Y, in this case 1.0. The string is terminated by a CRLF.

This example shows an output 12.45678 MHz.



Horizontal Close-Up View



De-populated Board Close-Up (no through-hole components)

WARRANTY

NOVATECH INSTRUMENTS, INC. warrants that all instruments it manufactures are free from defects in material and workmanship and agrees to replace or repair any instrument found defective during a period of one year from date of shipment to original purchaser.

This warranty is limited to replacing or repairing defective instruments that have been returned by purchaser, at the purchaser's expense, to NOVATECH INSTRUMENTS, INC. and that have not been subjected to misuse, neglect, improper installation, repair alteration or accident. NOVATECH INSTRUMENTS, INC. shall have the sole right to final determination regarding the existence and cause of a defect.

This warranty is in lieu of any other warranty, either expressed or implied, including but not limited to any warranty of merchantability or fitness for a particular purpose. In no event shall seller be liable for collateral or consequential damages. Some states do not allow limitations or exclusion of consequential damages so this limitation may not apply to you.

All instruments manufactured by NOVATECH INSTRUMENTS, INC. should be inspected as soon as they are received by the purchaser. If an instrument is damaged in shipment the purchaser should immediately file a claim with the transportation company. Any instrument returned to NOVATECH INSTRUMENTS, INC. should be shipped in its original shipping container or other rigid container and supported with adequate shock absorbing material.

This warranty constitutes the full understanding between NOVATECH INSTRUMENTS, INC. and the purchaser and no agreement extending or modifying it will be binding on NOVATECH INSTRUMENTS, INC. unless made in writing and signed by an authorized official of NOVATECH INSTRUMENTS, INC.

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