INSTRUMENTS, INC.

Precision 350 MHz Signal Generator

Model 425A

The 425A is a Precision 350 MHz Frequency and Phase Agile Synthesized Signal Generator in a small shielded table top case. The 425A generates Sine, LVCMOS, and LVDS output signals simultaneously up to 350 MHz in 10 µHz steps under control from a serial port. Multiple 425A can be synchronized and used to generate the signals needed for radar, acoustic testing and similar applications. The 425A comes with a ±1.5ppm on-board TCXO clock. When using an external clock source, the 425A has the same accuracy and stability as the clock and remains phase synchronous with other units operated from the same source.

Specifications:

OUTPUTS

TYPES: Sine, LVDS and LVCMOS simultaneously.
IMPEDANCE: 50 Ω. (100 Ω differential for LVDS)
RANGE: 250 kHz to 350 MHz with 10 µHz resolution (internal clock).
SINE AMPLITUDE: full scale approximately +7 dBm (0.50 Vrms) into 50 Ω load. Settable from 0.14 to 0.50 V_{rms} by the "V0" command. (14-bit DAC). ±3dB referenced to amplitude at 100 MHz.

LVCMOS AMPLITUDE

V_{OL}<0.5 V, V_{OH}>2.0 V into a series-terminated load.
$T_{r,f}$ <2.5 ns. Duty Factor: 40-60% (divider off). 50 Ω. Programmable 16-bit divider with a selectable /2 prescaler allows LVCMOS frequencies below 2 Hz. (LVCMOS optimized for frequencies <= 125 MHz)

LVDS AMPLITUDE

Meets EIA-644A specifications when terminated into a 100 Ω differential load (driver: SN65LVDS100, or equivalent).

CONTROL

Output frequency (48-bits), phase (14-bits), CMOS divider, and amplitude scaling (10-bits) are controlled by a serial port. Settings can be saved in EEPROM.

ACCURACY AND STABILITY

Accuracy: < ±1.5ppm at 10-40 ^{o}C. Stable to an additional ±2ppm per year, 18-28 ^{o}C.

EXTERNAL CLOCK/REFERENCE IN

Direct external clock frequency range of 250 to 1000 MHz or locked to a 10.0 MHz (±0.01%) reference. The 425A specifications depend upon the quality of this signal.
Input Level (50 Ω).**:**
10 MHz Reference: 0.75-1.25 Vrms Sine or LVCMOS Square Wave.
External Clock: -3 to +6 dBm sine wave.

SPECTRAL PURITY (Typical, 50 Ω load, int. clock)

Phase Noise:	<-140 dBc, 10 kHz offset, 10 MHz out.
Spurious:	<-70 dBc below 10 MHz
	<-60 dBc below 50 MHz
	<-55 dBc below 150 MHz
	<-45 dBc below 350 MHz
Harmonic:	<-65 dBc below 1 MHz
	<-60 dBc below 10 MHz
	<-55 dBc below 25 MHz
	<-45 dBc below 50 MHz
	<-40 dBc below 150 MHz
	<-25 dBc below 350 MHz

POWER REQUIREMENTS

+4.75 to +5.25 V @ <750 mA. 2.5 mm center-positive connector on rear panel. AC line (country dependent) adapter provided.

SIZE

39 mm H, 107 mm W, 172 mm L, not including connectors.

CONNECTORS

BNCs for SINE Out, LVCMOS Out, LVDS out, EXT CLK In. 2.5 mm center-positive for power. DE-9 for serial.

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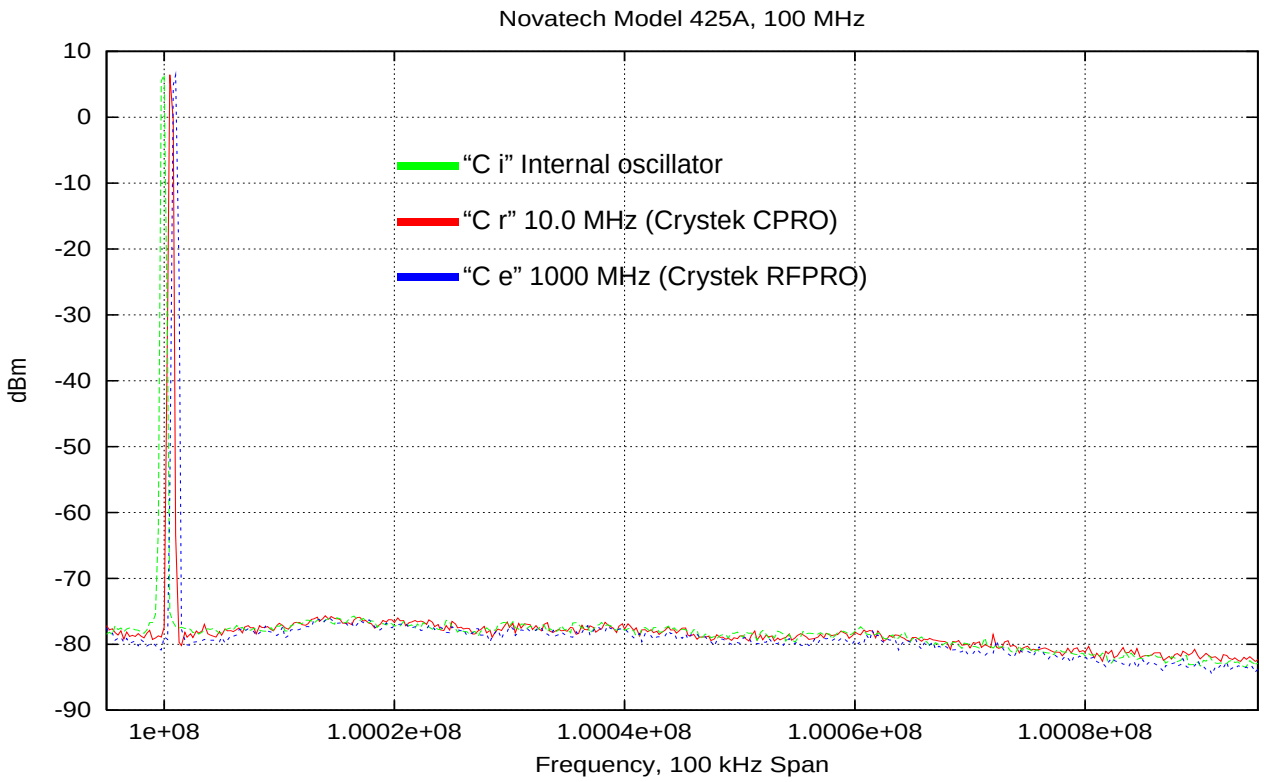
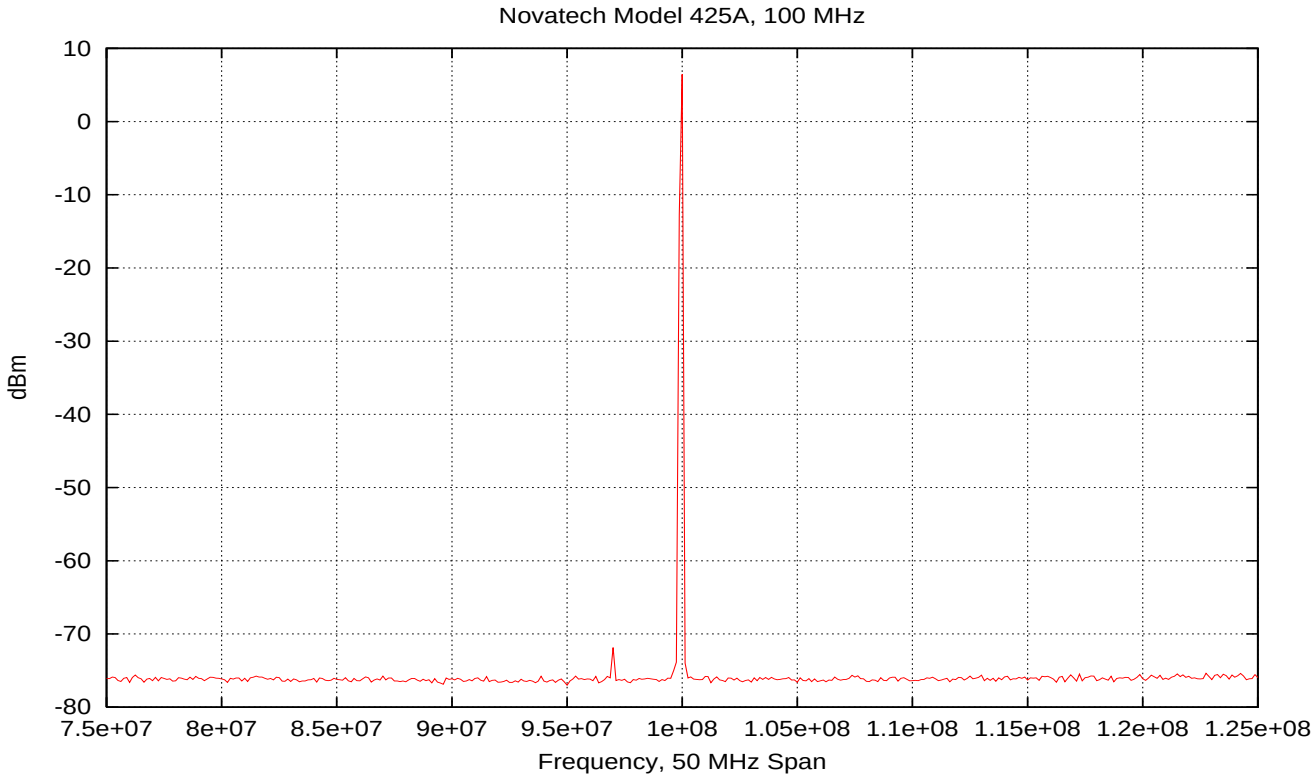
NOVATECH INSTRUMENTS, INC.
P.O. Box 55997
Seattle, WA 98155-0997
United States of America
http://www.novatech-instr.com/
sales@novatech-instr.com
206.363.4367 FAX/206.301.8986 Voice

Table 2: Serial Commands

Serial Command	Function
F0 xxx.xxxxxxxxxx	Set **F**requency of output in MHz to nearest 10 μHz. Decimal point required.
P0 N	Set relative **P**hase of output sinewave. N is an integer from 0 to 16383. Phase is set to N*360^{o}/16384 or N*2π/16384 radians. This is useful when multiple Model 425A are running from the same clock source.
E x	Serial **E**cho control. x=D for Echo **D**isable, x=E for Echo **E**nable. Disable echo for maximum serial port speed.
C x	Select **C**lock source. x=E for **E**xternal clock input 250 MHz to 1000 MHz, x=I for **I**nternal temperature compensated reference, or x=R for external 10 MHz **R**eference. The quality of the external input affects the specifications of the 425A. The "F0" command requires scaling (see manual) when clocks other than the internal clock are used.
R	**R**eset. This command resets the 425A. EEPROM data is preserved and, if valid, is used upon restart. This is the same as cycling power.
CLR	**Cl**ea**r**. This command clears the EEPROM valid flag and restores all factory default values.
A x	x=E for LVCMOS **E**nable, x=D for LVCMOS **D**isable. Default value is "**D**"
D0 N	Set **D**ivider value on LVCMOS output. N is an integer from 0 to 65535. The output frequency set by the "F0" command is divided by N+1 before being sent to the LVCMOS driver. Duty cycle varies with divide ratio.
PR x	x=E for Enable **Pr**escaler, x=D for Disable Prescaler. When enabled, the frequency set by the "F0" command is divided by 2 before entering the LVCMOS divider specified by the "D0" command. This allows a maximum divide integer of 131072.
S	**S**aves current state into EEPROM and sets valid flag. State used as default upon next power up or reset. Use the "CLR" command to return to default values.
QUE	Return present frequency, phase and status. Returns a character string of all internal settings.
M N	**M**ode command. Mode 'M 0' is single tone.
V0 N	Set **V**oltage level of output. In default, the amplitude is set to the maximum of approximately 0.5 V_{rms} (+7 dBm) into 50 Ω (default N = 1023). N can range from 0 to 1023 (no decimal point allowed). Voltage level is scaled by approximately: ***0.27 + 0.19*N/264*** If N >1023, the command is ignored and the level remains at its previous setting. (range is approximately 0.15 V_{rms} to 0.5 V_{rms})
I x	Set the **I**/O update pulse method. If x=a, then an I/O update is issued **a**utomatically at the end of each serial command (default). If x=m, then a **m**anual I/O update pulse is expected to be sent by a subsequent 'I p' command.
B aabb[cc[dd[ee[ff[gg[...]]]]]]	This **B**yte command allows each register in the DDS chip to be set. Different registers require a various number of bytes to be written depending upon the instruction word "aabb". All values are in hexadecimal and no error checking, other than correct format, is performed.


Novatech Model 425A, 100 MHz
"C i" Internal oscillator
"C r" 10.0 MHz (Crystek CPRO)
"C e" 1000 MHz (Crystek RFPRO)
dBm
10
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
1e+08
1.0002e+08
1.0004e+08
1.0006e+08
1.0008e+08
Frequency, 100 kHz Span


Novatech Model 425A, 100 MHz
dBm
10
0
-10
-20
-30
-40
-50
-60
-70
-80
7.5e+07
8e+07
8.5e+07
9e+07
9.5e+07
1e+08
1.05e+08
1.1e+08
1.15e+08
1.2e+08
1.25e+08
Frequency, 50 MHz Span