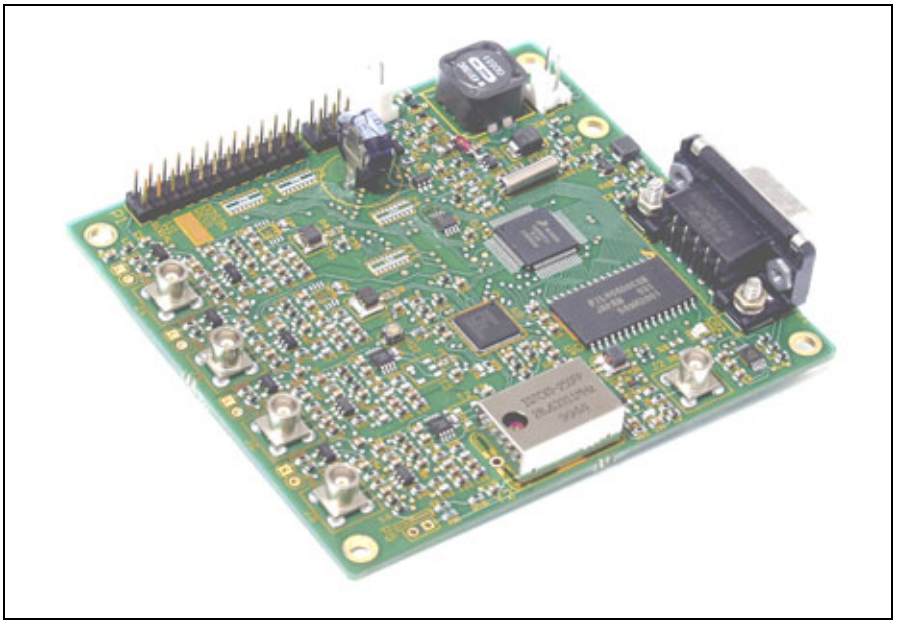
NOVATECH
INSTRUMENTS, INC.

INSTRUCTION MANUAL
Model DDS9m 170MHz 4-Channel Signal Generator Module



DDS9m

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1.0 DESCRIPTION

1.1 The Model DDS9m is a four-channel **D**irect **D**igital **S**ynthesizer (DDS) on a small printed wiring module with RS232 serial control. The DDS9m provides four independent sine wave and LVCMOS output signals, which can be set from 0.1Hz to 171MHz in 0.1Hz steps when using the internal VCTCXO clock (LVCMOS is optimized for outputs greater than 1MHz and less 125MHz).

1.2 The DDS9m can also be used with an External Clock input. An on-board programmable frequency multiplier generates the master clock allowing user configured frequency ranges. The multiplier can be disabled for direct inputs up to 500MHz for optimum phase noise performance. When used with the same external clock source, multiple DDS9m are phase synchronous.

2.0 SPECIFICATIONS

2.1 OUTPUTS

TYPES: Four Sine and LVCMOS simultaneously (four frequencies.)
IMPEDANCE: Sine: 50Ω; LVCMOS: 50Ω.
RANGE: 0.1Hz to 171MHz in 0.1Hz steps (Sine out, int. clock).
SINE AMPLITUDE: approximately $1V_{pp}$ (+4dBm @ 35MHz) into 50Ω. Programmable from 0/1024 to 1023/1024 of Full Scale (10-bits).
PHASE: Each channel 14-bits programmable.
FLATNESS: ±3dB from 1kHz to 150MHz referenced to amplitude at 35MHz, full scale.

2.2 LVCMOS AMPLITUDE

V_{oh} >=2.4V and V_{ol} <=0.4V when series terminated. Rise and fall times <1.5ns. (1MHz< F_{out}<125MHz)

2.3 CONTROL

Output frequencies, amplitudes (10-bits) and phases (14-bits) are controlled by an RS232 serial port at 19.2kbaud. All settings (except table mode data) can be saved in non-volatile (EEPROM) memory via the RS232 port.

2.4 ACCURACY AND STABILITY

Accuracy: <±1.5ppm at 10 to 40^{o}C. Stable to an additional ±1ppm per year, 18 to 28^{o}C. (Internal Clock)

2.5 EXTERNAL CLOCK IN

LEVEL: 0.2 to 0.5Vrms Sine or Square Wave. 50Ω.
FREQUENCY: 10MHz to 125MHz with multiplier of 4 to 20 enabled. Direct input of 1MHz to 500MHz.

2.6 SPECTRAL PURITY (Typ. 50Ω load, internal clock, full-scale output)

Phase Noise: <-120dBc, 10kHz offset, 5MHz out.
Spurious: <-60dBc below 10MHz (typ. 300MHz span)
<-60dBc below 40MHz
<-55dBc below 80MHz
<-50dBc below 160MHz
Harmonic: <-65dBc below 1MHz
<-55dBc below 20MHz
<-45dBc below 80MHz
<-35dBc below 160MHz
(channel-channel isolation: <-60dBc)

2.7 TABLE MODE

On-board 4Mb static ram holds up to 32,768 profile points in table mode allowing a different output in 100µs increments. Channels 0 and 1 only.

2.8 POWER REQUIREMENTS

+3.14V to +3.46VDC@<750mA. Battery back-up 3.0V nominal at <400µA (2-AA, LR6, typical).

2.9 SIZE

82.6mm by 88.9mm circuit board. Max. height 10mm.

2.10 CONNECTORS

MCX for Sine Outputs and EXT CLK IN. 2-pin header for +3.3V power and external back-up battery. 24-pin header for high speed control. DE9 for Serial Control. 2-pin wire-points for LVCMOS outputs.

3.0 HARDWARE INSTALLATION

WARNING:

The DDS9m contains static sensitive components. Before opening the package, follow appropriate static precautions. Failure to follow static precautions may damage the DDS9m.

3.1 **Power Connection.** Figure 1, Connection Placement Diagram, shows a top view of the DDS9m module. The required power of +3.3Volts DC is applied through a 2-pin connector (mates with Amp 640621-2). If you are using a Novatech Instruments, Inc. supplied connector, Red is +3.3VDC and Black is the common return.

3.2 The quality of your power supply may affect the performance of the DDS9m. The supply should be free of ripple and noise (<50mV). Even though

extensive filtering is used on the DDS9m board, a quiet and well regulated power supply will ensure optimum performance. If switching power supplies are used, please verify that your system noise requirement is met.

3.3 **RS232 Installation.** To use the DDS9m in the RS232 mode, connect your host computer to the 9-pin female RS232 connector on the DDS9m. If you are using a PC, a 9-pin monitor extension cable used as an RS232 cable will allow direct connection to the DDS9m without the use of a null modem cable or gender changer. If you are using a different computer, terminal or other control source, please note that the data **TO** the DDS9m is on pin 3; the data **FROM** the DDS9m is on pin 2 and the **COMMON** return is on pin 5. Set your host to 19.2 kbaud, 8 bits, 1 stop bit, no parity and no hardware flow control. See Table 2 for RS232 Serial Commands.

3.4 You may use a USB to RS232 adapter cable with computers that do not provide a serial port. Follow the manufacturer's installation instructions when using a USB adapter.

3.5 Commands are not case sensitive. There must be a space after each command except `R`, `CLR`, `S` and `QUE`. End with any combination of `CR`, `LF` or `CRLF`. Illegal commands will result in an error code being returned per Table 1.

Table 1: RS232 Error Codes

Error Code	Meaning
`OK`	Good command received (not sent for R, CLR and QUE)
`?0`	Unrecognized Command
`?1`	Bad Frequency
`?2`	Bad AM Command
`?3`	Input line too long
`?4`	Bad Phase
`?5`	Bad Time
`?6`	Bad Mode
`?7`	Bad Amp
`?8`	Bad Constant
`?f`	Bad Byte

3.6 The `"QUE"` command returns five hexadecimal strings reflecting the present state of the DDS9m. See page 9 for an explanation of the values that make up these strings. Note that the frequency settings will be scaled as discussed below if an external clock is used.

3.7 The ***"B"*** command can cause erroneous operation and must be used with care. Detailed knowledge of the operation of the Analog Devices AD9959 DDS generator is required. Since all registers are accessible, it is possible to set the board into a non-functional mode, requiring a reset. Application Note AN001 shows an example of the command for setting frequency.

NOTE:

*The program **SOF8** is available for the DDS9m. This program provides a graphical interface for all the serial commands, allowing simple control of the DDS9m. The **SOF8** CD contains multiple versions of the software. Be sure to read the README file to see which is appropriate for your instrument.*

3.8 **Internal Clock.** If you plan to use the DDS9m internal clock, which is the default setup mode, no action is required. If the DDS9m was previously set to use the external clock, send the serial command `"C i"` to reselect the internal clock. If you wish to maintain this setting, use the save command `"S"`.

3.9 **External Clock**. If you are providing your own clock source, send the serial command `"C e"`. Apply your clock to the External Clock Input MCX on the board. Note that phase noise and stability are dependent upon your supplied clock. See specifications for signal levels required and acceptable frequency range. If you wish to maintain this setting, use the save command `"S"`.

3.10 The external clock can also be used with Kp=1 for direct connection to the DDS generator. With Kp=1, the PLL multiplier is disabled. Use this direct input, up to 500MHz, for optimum phase noise performance.

NOTE:

When using an external clock, frequency scaling of the `"Fn"` command may be required. Please see Operation, Section 4, for details.

Table 2: RS232 Serial Commands

RS232 Command	Function
`Fn xxx.xxxxxxx`	Set Frequency of output "n" in MHz to nearest 0.1Hz. Decimal point required. n=0, 1, 2, 3. Maximum setting: 171.1276031MHz. Single tone mode.
`Pn N`	Set Phase of output "n." N is an integer from 0 to 16383. Phase is set to N*360^{o}/16384 or N*π/8192 radians. Sets the relative phase of the frequency output depending upon the value of n=0, 1, 2, 3. Single tone mode.
`E x`	Serial echo control. x=D for Echo **D**isable, x=E for Echo **E**nable
`C x`	Select clock source. x=E for **E**xternal clock, x=I for **I**nternal Clock. May require adjustment of Kp and external filtering of output when an external clock is used.
`R`	Reset. This command resets the DDS9m. EEPROM data is preserved and, if valid, is used upon restart. This is the same as cycling power.
`CLR`	Clear. This command clears the EEPROM valid flag and restores all factory default values.
`A x`	CMOS output control. x=E for LVCMOS **E**nable, x=D for LVCMOS **D**isable.
`S`	Saves current state into EEPROM and sets valid flag. State used as default upon next power up or reset. Use the `"CLR"` command to return to default values.
`QUE`	Return present frequency, phase and status. Returns a character string of all internal settings.
`M N`	Mode command. Mode '0' is single tone on all channels (default). If N=a, then the phase is automatically cleared during each command; if N=n, then the phase is not cleared (default). See Section 4 for details.
`Vn N`	Set voltage level of output "n." In default, the amplitude is set to the maximum: approximately 1V_{pp} (+4dBm) into 50Ω. N can range from 0 (off) to 1023 (no decimal point allowed). Voltage level is scaled by N/1023. n=0, 1, 2, 3 to set the amplitude on frequency 0, 1, 2 or 3. If N >=1024, the scaling is turned off and the selected output is set to full scale.
`Vs N`	Set the output scaling factor. N=1 for full scale, N=2 for half scale, N=4 for one quarter scale and N=8 for one eighth scale. All channels are scaled equally.
`Kp aa`	Set the DDS on-chip PLL reference multiplier constant. Must be one Hexadecimal byte as two characters. Legal values are 1 (bypass PLL) and 4 to 20 (01_h, 04_h to 14_h). Values of Kp times clock frequency must not be between 160MHz and 255MHz (for internal clock, this disallows 5<=Kp<= 9). (see paragraph 4.12 for other considerations)
`I x`	Set the I/O update pulse method. If x=a, then an I/O update is issued **a**utomatically at the end of each serial command (default). If x=m, then a **m**anual I/O update pulse is expected to be sent by a subsequent `'I p'` command. See section 4.
B aa[bb[cc[dd[ee[ff[gg]]]]]]	This **B**yte command allows each register in the DDS chip to be set. Different registers require a various number of bytes to be written depending upon the function. Please consult the Analog Devices AD9959 data sheet for details. Note that it is possible to set the DDS chip into a non-functional mode, requiring a power cycle to recover. All values are in hexadecimal and no error checking, other than correct format, is performed.

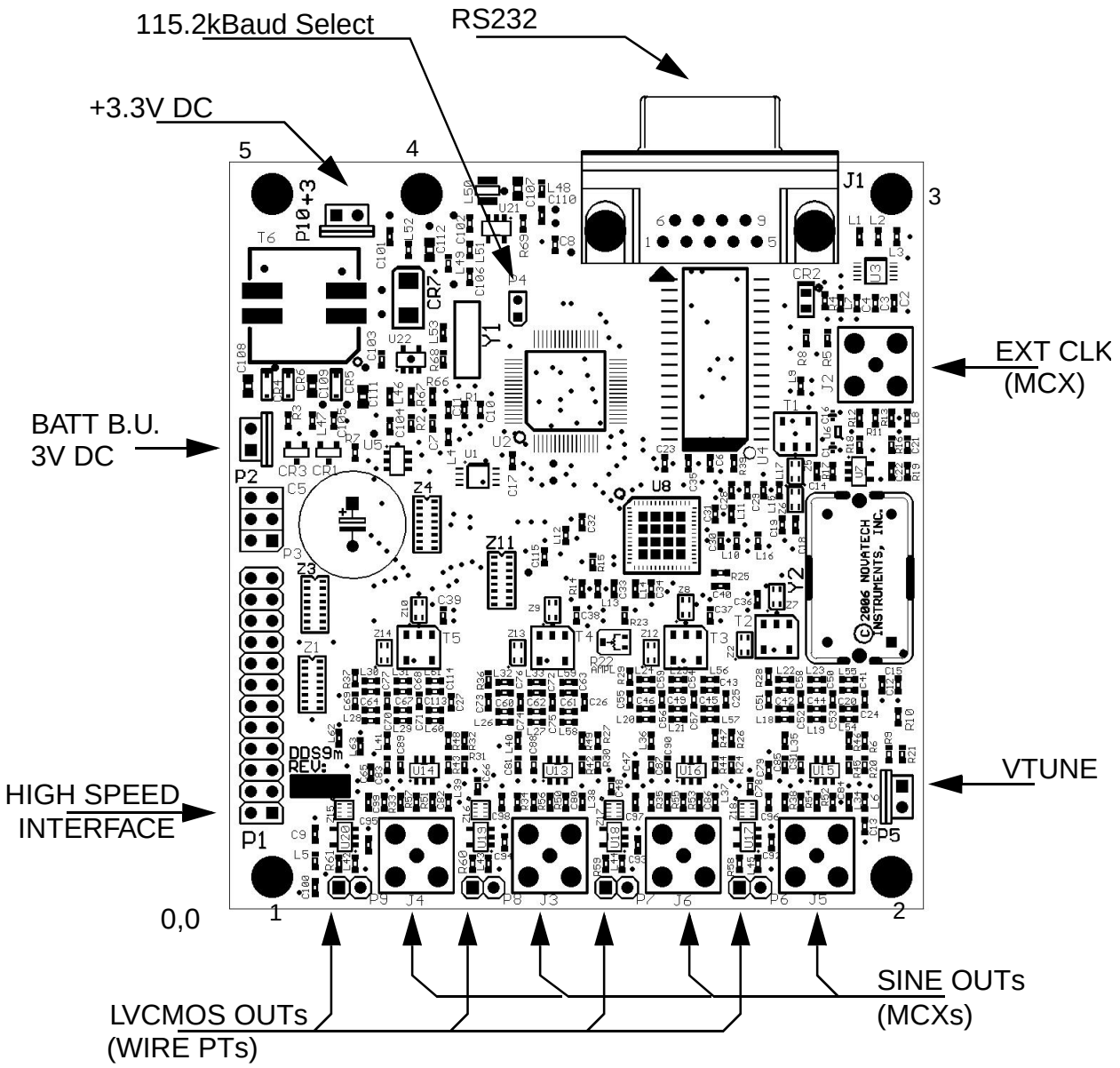

Figure 1: Component Placement

Table 3: Mounting Hole Locations

Hole (CCW)	X,Y mm	X,Y inch
1	5.08, 3.81	0.20, 0.15
2	78.7, 3.81	3.10, 0.15
3	78.7, 85.1	3.10, 3.35
4	22.9, 85.1	0.90, 3.35
5	5.08, 85.1	0.20, 3.35

Lower Left Corner of board (as shown by 0,0) is origin of X,Y coordinates for hole location.

Pin Number	Function	Type	Pin Number	Function	Type
1	Ground (Power Supply Common)	PS	2	+3.3 V (Power Supply Reference, 50mA max)	O
3	Ground (Power Supply Common)	PS	4	SER-	I
5	no connect	--	6	no connect	-
7	no connect	-	8	no connect	-
9	RES-	I	10	IRQ-	I/O
11	EN-	O	12	SDATA	I/O
13	SCLK	I	14	IOUD	I/O
15	SYNO	O	16	SYNI	I
17	no connect	-	18	P0	I
19	P1	I	20	P2	I
21	P3	I	22	SD3	I
23	SD2	I	24	SD1	I

Table 4: High Speed Interface Connector Pinout, P1.

WARNING:

The parallel inputs are 3.3V CMOS compatible. Applying 5V logic signals to these inputs will permanently damage the DDS9m. If your system is 5V, it is suggested that VHC buffers powered by 3.3V be placed between the DDS9m and your system. You may use the 3.3 V on pin 2 of P4 for this power (up to 50mA).

3.11 **High Speed Interface Installation.** The DDS9m can also be controlled by using connections to the 24-pin (12x2) header. See Table 4 for connector pinout and pin descriptions. Use of this port requires detailed knowledge of the AD9959 DDS generator IC. You can use the 'B' command to test your operation.

NOTE:

The table mode or table RAM is not accessible from the high speed port. The high speed port controls only the DDS ASIC.

NOTE:

For maximum interface speed, the high-speed inputs do not have additional protection against ESD damage beyond that provided by the CMOS inputs (+/-2kV, Human Body Model. +/-200 V, machine model) and 47Ω series resistors.

3.12 All of the inputs are 3.3V VHCMOS compatible and require:

V_{il} <= 0.4 volts

V_{ih} >= 2.7 volts

3.13 C_{in} on each pin is approximately 10pF (application cable capacitance not included). The input pins are series terminated with a 47Ω resistor. It is recommended that a series termination resistor of 50-100Ω be used at each signal line source to prevent reflections and ringing. The exact value will be determined by your application circuitry and cabling.

3.14 SER-, pin 4 of P1 must be held low to select the high-speed interface. During initialization, EN-, pin 11 of P1, is held high. When initialization is complete it returns low.

3.15 **Signal Outputs.** There are eight signal outputs on the DDS9m: four channels of Sine and the corresponding LVCMOS/TTL. The Sine outputs are provided on MCX connectors (Johnson Components, 133-3701-133 or equivalent) on the board edge. Simply connect your 50Ω application cable to appropriate output. The LVCMOS outputs are on wirepoints near the MCX outputs. The square pad is the LVCMOS output and the round pad is ground. If you are not using the LVCMOS/TTL output, it is suggested that it be disabled by sending the "A D" (default is disabled) command for best system noise performance.

3.16 **Mounting.** Five mounting holes are provided on the board. These holes are electrically connected to circuit common and may be used for shield connections. Clearance is provided for up to 3mm diameter screws. Please allow at least 3 mm clearance on the bottom side when mounting to a conductive chassis or case. Refer to Table 3 and Figure 1 for locations.

NOTE:

The DDS9m is cooled by convection. Verify that there is adequate free air flow around the board when mounting in an enclosure. Approximately 2 Watts are dissipated.

4.0 Operation

4.1 **Power on reset.** After power is applied, the DDS9m takes approximately 500ms to initialize. Commands sent during this time will be ignored or may cause erroneous operation.

4.2 Specifications are met within 15 minutes of power-up in stable environment.

4.3 After the DDS9m has been installed in the customer application system, all that is required for operation is to send the appropriate serial commands per Table 2.

4.4 The user host computer software must properly format the serial commands. Incorrect formatting will result in an error code being returned. See Table 1 for a list of error codes.

4.5 For maximum interface speed, it is suggested that Echoing be disabled by the "E d" command. This will allow the host to send characters at a faster rate. Note that no flow control is provided. Depending upon your host, the DDS9m may not be able to keep up with serial characters. The DDS9m will respond with an "OK" for a correctly received data command. You will have to verify correct operation at your host rate.

4.6 A special baud rate command is available if you wish to set a different baud rate. The value set by this command is volatile and not saved in EEPROM. Upon power up, reset or clear, the DDS9m defaults to 19.2kBaud.

```
Kb 78          ;9.6kBaud
Kb 3c          ;19.2kBaud
Kb 1e          ;38.4kBaud
Kb 14          ;57.6kBaud
Kb 0a          ;115.2kBaud
```

NOTE:

A jumper is provided to select 115.2kBaud as the default Baud Rate. Refer to Figure 1 for location. When the 2mm jumper is moved so the header pins are open, 115kBaud is selected. It is suggested that the jumper be left on a free pin for future use.

4.7 If you are using an external clock, the value sent to the DDS9m in the "Fn" command must be scaled. The output frequency of the DDS9m when used with an external clock is given by:

$$F_{out} = (F_{command})*(K_{pe}*F_{ext\ clk})/(K_{pi}*F_{int\ clk})$$

Where K_{pe} is the value of Kp set by the customer, and K_{pi} is the internal default Kp (0x0f).

4.8 The nominal Internal Clock has a value of 28,633,115.306666667Hz. Best performance is obtained when the External Clock input frequency times the Reference PLL multiplier (Kp) is close to the default value (429.4967296MHz, max: 500MHz), as the on-board low-pass filters are optimized for that range.

4.9 For an example of scaling, suppose an external clock of 10.000MHz is used and an output of 1.544MHz is desired, with $K_{pe}=K_{pi}=15$:

$$F_{command} = (1.544)*(15*28,633,115.306666667)/(15*10,000,000)$$
$$= 4.4209530$$

4.10 The command then sent to the DDS9m for the 1.544MHz output, with a 10MHz external clock, will be (assuming Kp is unchanged):

```
Fn 4.4209530
```

where 'n' is your selected channel

NOTE:

You must account for your clock frequency error and calculation roundoff when using an external clock.

4.11 Beginning with Software Revision 2.1, it is possible to control the internal range bit on the DDS ASIC.

4.12 For normal operation the Kp command is unmodified. However, if it is desired that the clock multiplier gain bit be set HIGH (for Kp*[Ext Clk Freq] from 255 and 500 MHz), add hexadecimal 0x80 to the Kp value to be set. For the bit to be forced LOW (100 to 160 MHz), add hexadecimal 0x40 to the Kp value to be set.

4.13 Since the resolution of the DDS9m is 32-bits, the typical fractional frequency error (**Δf/f)** for output frequencies in the MHz range will be less than 0.1ppm, even when exact values are not possible.

Typical Δf/f for External Clock of 10.0MHz

Kp	Desired Fout	Command	Δf/f
15	1.544MHz	`Fn 4.4209530`	2.19×10^{-8}
20	1.544MHz	`Fn 3.3157148`	1.43×10^{-8}
15	2.048MHz	`Fn 5.8640620`	1.45×10^{-8}
20	2.048MHz	`Fn 4.3980465`	2.02×10^{-8}

NOTE:

*The "**B**" command can be used to test AD9959 DDS chip programming as it allows access to all internal registers. While not a real-time simulation, each "**B**" command functions as an input by putting a data byte directly into the AD9959 via an SPI port, and then pulses the IOUD line. This is similar to a procedure that a customer control circuit might perform. The "B" command values are not saved in RAM, so they will not show in the "QUE" command output nor can they be saved in EEPROM. Consult the Analog Devices AD9959 data sheet for detailed information regarding the internal AD9959 register functions.*

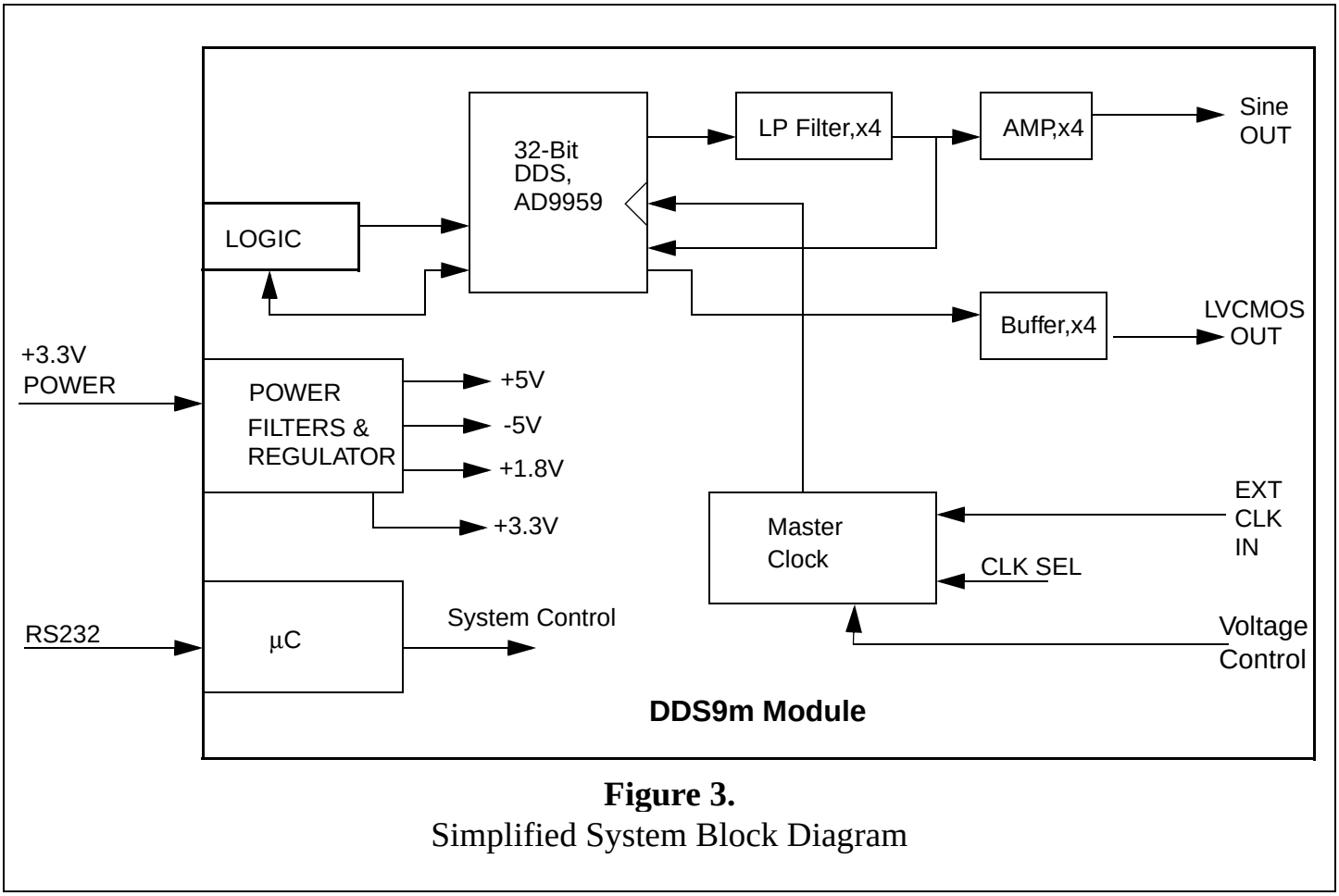

Figure 3.
Simplified System Block Diagram

"Que" command output (all values are hexadecimal) values:

```
05F5E100 0000 0000 03FF 00000000 00000000 000301
05F5E100 0000 0000 03FF 00000000 00000000 000301
05F5E100 0000 0000 03FF 00000000 00000000 000301
05F5E100 0000 0000 03FF 00000000 00000000 000301
80 BC0000 0000 6102 21
```

Description:
Line 1: "05F5E100", frequency in 0.1Hz steps per LSB; "0000", phase setting; "03FF", amplitude setting (default is scaling off); "0000", linear ramp rate; "00000000", rising delta frequency; "00000000", falling delta frequency, "000301", channel function register.

The last line gives the status of AD9959 registers and internal software registers: "80", channel select register (CSR); "BC0000", function register 1 (FR1); "0000", function register 2 (FR2); "6102", internal µC control registers; "21", software revision as x.y, Rev 2.1 in this example. Consult the Analog Devices AD9959 data sheet for meaning of registers. Each line is terminated by a carriage return/line feed (CRLF) pair.

4.14 Phase relationships are maintained by appropriate use of the "M" and "I" commands. The "M" command has special modes "M a" and "M n". "M a" means automatically clear phase at the end of each command. This will clear the phase register each time any command is performed. This is important when all outputs must be phase aligned. However, it may cause a phase discontinuity in the output.

4.15 The "M n" command turns off the automatic clearing of the phase register. This is the default mode. In this mode, the phase register is left intact when a command is performed. Use this mode if you want frequency changes to remain phase synchronous, with no phase discontinuities.

4.16 Further control of phase relationships and timing of command execution can be exercised by using the "I m", "I a" and "I p" commands. The default mode is "I a" in which a command is parsed and executed immediately following the end of the serial input sequence. In the "I m" mode, an update pulse will not be sent to the DDS chip until an "I p" command is sent. This is useful when it is important to change all the outputs to new values simultaneously.

4.17 For applications which require precise amplitude matching between the channels, the recommended method is to use the "Vn N" command to adjust the channels to match the other. This command provides 10-bits of adjustment range.

4.18 **High Speed Interface Operation.** When the high speed interface (P1) mode is chosen, the operation of the DDS9m is completely dependent upon the user supplied interface circuitry. The on-board microprocessor and software are disabled in parallel operation. Therefore, no error conditions are detected or reported.

NOTE:

The AD9959 pins MASTER_RESET, PWR_DWN_CTL, CS are set by the on-board microcomputer at power-up and are not accessible on the high speed interface. The table mode or table RAM is not accessible from the high speed interface.*

4.19 The on-board Voltage Controlled Temperature Compensated Crystal Oscillator (VCTCXO) can be adjusted approximately +/-5ppm from nominal by applying a 0 to 5Volt signal on P5. Your voltage control must be capable of sourcing and sinking 0.5mA. Nominal voltage is approximately 2.5 Volts. This feature is useful for applications which require Phase Locking to external sources, using customer supplied circuitry.

4.20 **Other Modes**. The DDS9m can be programmed by using the "B" command to perform many other outputs. The "B" command can be used to gain control over the on-board AD9959 DDS ASIC. Refer to the Analog Device data sheet for detailed information when using the "B" command.

5.0 Theory of Operation

5.1 Please refer to the simplified System Block Diagram in Figure 3 for the following discussion.

5.2 At every cycle of the DDS9m master clock, the 32-bit DDS integrated circuit increments the phase of an internal register by a value determined by the frequency setting loaded into the on-chip registers. This digital phase value is converted on-chip to a sinusoidal amplitude level and delivered to on-chip 10-bit digital-to-analog converters. The analog signals from these converters are filtered by differential 7th-order elliptical low pass filters, amplified and sent to the MCX receptacles.

5.3 The frequency generated by the DDS IC is determined by the 32-bit frequency word loaded into the frequency register on the DDS9m. The output frequency is given by:

$$F_{out} = F_{setting} * Kp * F_{clock} / 2^{32} \text{ Hz}$$

Where: F_{clock} = 28,633,115.306666667 Hz (int.)
$F_{setting}$ = Binary value in DDS IC.
($F_{setting}$ ranges from 0 to 2^{31}-1)
Kp = PLL Multiplier (1 or 4 to 20)

This reduces to:

$$F_{out} = F_{setting} \text{ MHz}$$

for the internal (default) clock and the default PLL Multiplier (Kp=15) settings.

5.4 Since the DDS IC is a sampled data system, the output frequency is limited to a maximum of 1/2 the system clock frequency ($F_{setting}<=2^{31}-1$). While it is possible to generate an output near 50% of the clock, the distortion may be unacceptable. Therefore, the output is limited to approximately 40% of the system clock and steep output filters are provided on board: in this case 7th-order elliptical low pass filters.

5.5 If you are using an external clock and a Kp which give a clock substantially lower than the 429.497MHz default internal clock, you may need to filter the Outputs to obtain acceptable distortion for your application. For best performance, set the corner frequency at 40% or less of your external clock frequency times Kp. The lower your filter as a percentage of your clock frequency, the lower the distortion.

NOTE:

Since filtering occurs before the signal is level shifted to LVCMOS, the LVCMOS outputs may be erratic or distorted when using low clock frequencies. If you require an LVCMOS level signal when using low clock frequencies, it is recommended that you use an external comparator or level shifter connected to the output of your external filter.

5.6 For example, if you are using a 10MHz external clock, with the default reference multiplier (Kp) of 15, then the internal clock is 150MHz. An optimal filter for this frequency would then be approximately 60MHz (40% of 150MHz).

NOTE:

Per the Analog Devices AD9959 data sheet, your value of Kp times your selected clock frequency must not be between 160MHz and 255MHz. For the internal clock, values of Kp from 5 to 9 should not be used. You may also need to set the "VCO gain control" bit in register FR1 as indicated by the AD9959 data sheet. See paragraph 4.12.

6.0 PERFORMANCE TEST

6.1 Install the DDS9m as directed in the Serial Operation part of Section 3. Connect your host controller and operate the DDS9m per Section 4. The test limits assume a stable environment of 18-28^{o}C.

NOTE:

Allow the DDS9m to warm up for at least 15 minutes before performing any measurements. For best results, the DDS9m should be verified in its installed environment.

6.2 See Table 3 for a list of recommended test equipment to perform the following measurements.

Table 3: Recommended Test Equipment

Item	Minimum Specification	Recommended
Oscilloscope	300MHz, 50Ω	Tektronix TDS3032B
50Ω Termination	50Ω, ±1%	Tektronix 011-0049-01
Frequency Counter	180MHz	HP53132A
Counter Time Base	10MHz, <±0.1ppm	Novatech Instruments Model 2960AR
External Clock	400MHz	Novatech Instruments Model 440A

6.3 **Verify Frequency Accuracy.** To verify the frequency of the DDS9m, set the output sequentially to each value in Table 4, with the clock source set to internal. Connect the recommended frequency counter set to 50Ω termination and 0.1Hz resolution. Verify the limits show in Table 4. Test all channels to verify functionality of all outputs. If you do not use an external reference for the frequency counter, be sure to add the error of your counter to the tolerance. (LSD = **L**east **S**ignificant **D**igit on counter).

Table 4: Frequency Test Points

Frequency	Tolerance
100 kHz	±0.15 Hz ±1 LSD
1 MHz	±1.5 Hz ±1 LSD
10 MHz	±15 Hz ±1 LSD

Table 4: Frequency Test Points

Frequency	Tolerance
30 MHz	±45 Hz ±1 LSD
50 MHz	±75 Hz ±1 LSD
100 MHz	±150 Hz ±1 LSD
170 MHz	±255 Hz ±1 LSD

6.4 **Sine Out Amplitude Verification.** Set the frequency of the DDS9m to 10MHz. Connect the DDS9m to the oscilloscope set for 50Ω termination. Set the oscilloscope to measure to amplitude using at least 16 averages. Verify a reading of 1Vpp ±0.25Vpp. Repeat for the other outputs.

6.5 **Level Command Test.** Leave the output frequency set to 10MHz. Send the commands `"Vn 512"` to each channel, where `'n'` is your selected channel number. Verify that the amplitude on each channel decreases by one-half. Send the `"R"` command to reset the levels before performing the next tests.

6.6 **Output Flatness Verification.** Verify that the outputs are flat with frequency by performing the following test: Connect the DDS9m to the oscilloscope set for 50Ω termination. Use the same settings as Sine Out Amplitude Verification. Note the voltage reading.

6.7 Set the DDS9m to the values of Table 4. Verify that the oscilloscope amplitude reading remains within ±3dB (1.414 to 0.707) of the value noted in the previous paragraph. (limit upper frequency to150MHz)

6.8 Repeat the output flatness verification test for each output.

6.9 **External Clock Input Verification.** Set the frequency output to 10.000MHz by sending the command `"F0 10.7374182"` (scaled per section 4.0). Connect a 400MHz external clock source via a short coaxial cable to the external clock MCX. Send the command `"Kp 01"`. Send the command `"Ce"` to select the external clock input.

6.10 Verify an output of 10.0000000MHz, ±0.1Hz. You must account for any frequency errors in your external clock source.

6.11 Return the DDS9m to normal operation and default values by sending the `"CLR"` command.

6.12 This concludes the verification test of the DDS9m.

7.0 CALIBRATION

7.1 The DDS9m has two adjustable components: Y2, frequency, and R22, output amplitude. Calibration should be performed only if the DDS9m fails the performance test or if the unit has been repaired. Routine adjustments are not recommended nor generally required. This procedure assumes that the DDS9m has failed the performance test or has been repaired.

7.2 Before proceeding with calibration, send the `'CLR'` command to set the DDS9m to factory default values.

WARNING:

Calibration should be performed only by qualified personnel. The on-board components are static sensitive.

7.3 The adjustments shown are set to 1/2 the specification values.

NOTE:

Allow the DDS9m to warm up for at least 15 minutes before performing any adjustments. For optimum performance the DDS9m should be calibrated in an environment similar to its installation.

7.4 **Frequency Adjust, Y2.** Set the output of the DDS9m to 10.0000000MHz using the command `"F0 10.0000000"`. Connect output of channel 0 to your frequency counter set for 50Ω termination. Adjust Y2 using a non-metallic adjustment tool for 10.000000MHz, ±7.5Hz.

7.5 **Amplitude Adjust, R22.** Connect the output of channel 0 to the oscilloscope set to measure amplitude, with a minimum of 16 averages. Set for 50Ω termination. Set the output to 35MHz by sending the command `"F0 35.0000000"`. Adjust R22 for 1.00Vpp ±0.05Vpp. This completes the calibration of the Model DDS9m.

8.0 Appendix A. Table Mode Details.

8.1 The Model DDS9m contains on-board static RAM capable of storing up to 32,768 profile points. Each point contains phase, frequency, amplitude and dwell time information. The on-board microcomputer reads this RAM and programs the DDS ASIC per the profile point data. The profile can be set to loop continuously or to hold at the last point, until interrupted by a subsequent command.

NOTE:

Channels 0 and 1 can be set with the table mode.

8.2 The table mode is toggled on and off by an `'M t'` command from the serial port and executes customer provided profile points. `'M 0'` always turns off the table and returns to single tone mode. The DDS9m starts execution of the profile immediately upon a receipt of `'M t'` following an `'M 0'`.

8.3 The command sequence (**bold**) is of this form (comments after the ';' are not sent to the DDS9m, but are here for explanation purposes):

```
M 0
                ;turns off running table mode
t0 0000 aabbccdd,eeff,gghh,ii
                ;F0 profile point 0, on output 0
t1 0000 aabbccdd,eeff,gghh,ii
                ;F1 profile point 0, on output 1
t0 0001 aabbccdd,eeff,gghh,ii
                ;F0 profile point 1
t1 0001 aabbccdd,eeff,gghh,ii
                ;F1 profile point 1
...
t0 3fff aabbccdd,eeff,gghh,ii
                ;F0 profile point 0x3fff
t1 3fff aabbccdd,eeff,gghh,ii
                ;F1 profile point 0x3fff
M t
                ;begin execution of table
```

;`'0000'` two byte RAM address, T0 and T1 must be paired with same address
;`'aabbccdd'` four bytes frequency, hexadecimal, MSB first, 4 bytes. 0.1Hz resolution on LSB
;`'eeff'` phase offset, hexadecimal, MSB first, only 14-bits active, top two bits are ignored
;`'gghh'` amplitude scale, MSB first, only 10-bits active. Amplitude is scaled per above.
;`'ii'` dwell time, MSB first, in increments of 100µs. 0x00=loop back to start, 0xff=hold present setting. Each T0-T1 pair must have the same dwell.

8.4 The `','` (comma) in each record is used as a delimiter and must be included as shown. The inputs are not case sensitive. Subsequent `'M t'` commands will toggle the execution of the table on and off. Upon execution of the table, the output will always begin with address 0000 and progress until it encounters an 0xff or 0x00 in a dwell position. The last record in a table mode will be executed for 100µs if the dwell is set to 00.

NOTE:

Each record must be terminated with an 0x00 or 0xff in the dwell position to indicate the end of your data.

8.5 The current values stored in RAM can be read back by the `"Dn aaaa"` command. N=0 or 1 and "aaaa" is the address.

8.6 The RAM table is backed-up by a "supercap" for a minimum of 10 minutes. This allows for short power interrupts without losing the table information. A battery holder, with the appropriate connector, for two AA (LR-6) cells is provided with the DDS9m. These cells will retain the RAM for approximately one year with no power applied.

WARRANTY

NOVATECH INSTRUMENTS, INC. warrants that all instruments it manufactures are free from defects in material and workmanship and agrees to replace or repair any instrument found defective during a period of one year from date of shipment to original purchaser.

This warranty is limited to replacing or repairing defective instruments that have been returned by purchaser, at the purchaser's expense, to NOVATECH INSTRUMENTS, INC. and that have not been subjected to misuse, neglect, improper installation, repair alteration or accident. NOVATECH INSTRUMENTS, INC. shall have the sole right to final determination regarding the existence and cause of a defect.

This warranty is in lieu of any other warranty, either expressed or implied, including but not limited to any warranty of merchantability or fitness for a particular purpose. In no event shall seller be liable for collateral or consequential damages. Some states do not allow limitations or exclusion of consequential damages so this limitation may not apply to you.

All instruments manufactured by NOVATECH INSTRUMENTS, INC. should be inspected as soon as they are received by the purchaser. If an instrument is damaged in shipment the purchaser should immediately file a claim with the transportation company. Any instrument returned to NOVATECH INSTRUMENTS, INC. should be shipped in its original shipping container or other rigid container and supported with adequate shock absorbing material.

This warranty constitutes the full understanding between NOVATECH INSTRUMENTS, INC. and the purchaser and no agreement extending or modifying it will be binding on NOVATECH INSTRUMENTS, INC. unless made in writing and signed by an authorized official of NOVATECH INSTRUMENTS, INC.

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